# Multiphase Buck Game Plan

## Problems/Changes

* IC power dissipation is too high
  + Can relieve this by either going down to 1 FET and a slightly lower frequency
  + Or by using a FET with a lower QGate
* Thermal reliefs on small passives are too thick
* Add in a way to break open each channel to measure output current
* Currently IC power losses may be making up the majority of power losses on the board.
* New FET – should only need one, place footprints for two
* New output caps – need low ESR ceramic
  + Need to be stable at intended temperature and frequency
  + Check temperature rise due to self heating by calculating capacitor rms current

## Testing

* Still need to test full load regulation
* Should test ripple across full range of loads
* Should test transient with larger change in load
* Overcurrent and overvoltage protection

## Current Performance

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Target** | **Current** | **Causes/Changes** |
| Line Regulation | <0.1% | <0.04% | None |
| Load Regulation |  | <0.3% |  |
| Output Ripple | 25mV | 304mV | Output caps or Inductor |
| Transient Response |  | 0.625V;425us |  |

## Improvements

* Load Regulation: reduce resistance of high-power traces – make em’ fat
* Ripple Voltage (Double check data sheet calculations):
  + More output capacitance
  + Higher switching frequency
  + Reduce inductor impedance in high-frequency operation
  + Reduce output capacitor impedance in high frequency operation
    - NPo capacitor
  + Reduce the switching-node voltage spike.
    - Adding a bootstrap resistor in series or an RC snubber circuit
  + If the output current is large, then go for a ferrite or inductor to induce more damping into the self-resonance.
  + Second stage output filter (LC filter) with low ESR output capacitors
    - Need to make sure sense lines are to the left of the LC filter so the sense lines are not disrupted by the filter
    - The corner frequency can’t be too low
    - Small inductance
  + Consider switching out electrolytics for ceramic (see data sheet)
  + **Low ESR ceramic capacitors are the easiest way to reduce output ripple**
    - ESR inhibits a capacitor’s ability to quickly sink or source charge
  + Including some small ceramic additionally may help as well
  + Common mode filter
  + Need to check what the electrolytic capacitors ESR is at the expected, temperature and frequency.

## Take Aways/Actionable from Common Mistakes Doc

* Double check compensation loop calculations/design

## To-Do

1. Research which areas need improvement and outline steps which can be taken do improve them.
2. Learn what the compensation loop does and how it impacts transient response.
3. Learn what factors affect transient responses, what are the benefits and draw backs of having a faster vs. slower transient response and how to make those changes.